What Is Claimed Is:

1. A data processor including a plurality of registers usable for instruction execution and having an instruction set including a plurality of predetermined data transfer instructions,

wherein the predetermined data transfer instructions include a register specification field of plural bits in which the number of one register is explicitly specified from a group of registers, and

wherein the predetermined data transfer instructions specify data transfers between registers corresponding to numbers equal to or greater than, or equal to or smaller than a number specified in the register specification field and memory.

2. The data processor according to claim 1,

wherein the group of registers includes general purpose registers.

3. The data processor according to claim 2,

wherein the group of registers includes a procedure register in which a return address from a subroutine is stored when the subroutine is called.

4. The data processor according to claim 1,

wherein the predetermined data transfer

instructions include register indirectly addressing mode, and

wherein a register used in the register indirectly addressing mode is incremented or decremented for each transfer between the register and memory.

5. The data processor according to claim 4,

wherein a register used in the register indirectly addressing mode is a stack pointer.

6. The data processor according to claim 1,

wherein the predetermined data transfer instructions are 16-bit instructions.

7. The data processor according to claim 1,

wherein the predetermined data transfer instructions include a first store instruction specifying data transfers to memory from registers corresponding to numbers equal to or greater than a number specified in a register specification field as a starting point.

8. The data processor according to claim 1,

wherein the predetermined data transfer instructions include a first load instruction specifying data transfers from memory to registers corresponding to numbers equal to or greater than a number specified in a register specification field

as a starting point.

9. The data processor according to claim 1,

wherein the predetermined data transfer instructions include a second store instruction specifying data transfers to memory from registers corresponding to numbers equal to or smaller than a number specified in a register specification field as a starting point.

10. The data processor according to claim 1,

wherein the predetermined data transfer instructions include a second load instruction specifying data transfers from memory to registers corresponding to numbers equal to or smaller than a number specified in a register specification field as a starting point.

11. A data processor including an instruction control part for decoding instructions and controlling instruction execution sequences, and a plurality of registers,

wherein the instruction control part, when decoding a number specified in a register specification field of plural bits paired with specific operation code, controls data transfers between a group of registers corresponding to numbers equal to or greater than, or equal to or

smaller than the number, and memory.

12. The data processor according to claim 11, wherein the instruction control part can change the correspondence between numbers specifiable in the register specification field and registers according to setting states of a control register.

13. The data processor according to claim 11, wherein a group of registers specifiable by numbers of the register specification field includes general purpose registers.

14. The data processor according to claim 13, wherein the group of registers includes one or plural registers selected from a group of special-purpose registers other than general purpose registers within the data processor.